AF/4

PATENT
Customer No. 22,852
Attorney Docket No. 04329.1949-01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Atsushi YAGISHITA et al.	)	Group Art Unit: 2822
	)	
Application No.: 10/023,849	)	Examiner: Rose, Kiesha L.
	)	
Filed: December 21, 2001	)	Confirmation No. 4501
	)	
For: SEMICONDUCTOR DEVICE	)	

Attention: Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

TRANSMITTAL OF APPEAL BRIEF (37 C.F.R. 41.37)

Transmitted herewith is the APPEAL BRIEF in this application with respect to the Notice of Appeal filed on August 25, 2005.

This application is on behalf of

☐ Small Entity ☒ Large Entity

Pursuant to 37 C.F.R. 41.20(b)(2), the fee for filing the Appeal Brief is:

☐ $250 (Small Entity)

☒ $500 (Large Entity)

TOTAL FEE DUE:

Notice of Appeal Fee $0

Extension Fee (if any) $0

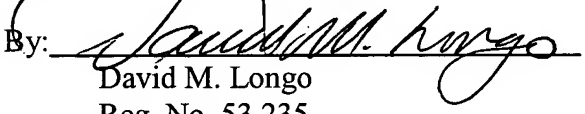
Total Fee Due $500

☒ Enclosed is a check for $500 to cover the above fees.

PETITION FOR EXTENSION. If any extension of time is necessary for the filing of this Appeal Brief, and such extension has not otherwise been requested, such an extension is hereby requested, and the Commissioner is authorized to charge necessary fees for such an extension to our Deposit Account No. 06-0916. A duplicate copy of this paper is enclosed for use in charging the deposit account.

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: November 17, 2005

By: 

David M. Longo
Reg. No. 53,235

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Sir:

APPEAL BRIEF UNDER RULE § 41.37

In support of the Notice of Appeal filed August 25, 2005, further to 37 C.F.R. § 41.37, Appellants present this brief and enclose herewith a check for the fee of $500.00 required under 37 C.F.R. § 41.20(b)(2).

This Appeal is filed to appeal the rejections of claims 38 and 39 set forth in the Office Action mailed June 3, 2005.

According to the Pre-Appeal Brief Conference Pilot Program (O.G. July 12, 2005), this brief is being timely submitted within one (1) month of the October 17, 2005, mailing date of a Notice of Panel Decision from Pre-Appeal Brief Review.

If any additional fees are required or if the enclosed payment is insufficient, Appellants request that the required fees be charged to Deposit Account No. 06-0916.

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TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The real party in interest is Kabushiki Kaisha Toshiba, a corporation of Japan, the assignee of the entire right, title, and interest in the application.

II. RELATED APPEALS AND INTERFERENCES

There are currently no other appeals or interferences, of which Appellants, Appellants' legal representative, or Assignee are aware, that will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 38 and 39 are the subject of this appeal. Claims 30-39 remain pending and under current examination, with claims 30-37 standing allowed.

In the 06/03/2005 Office Action, the Examiner rejected claim 38 under 35 U.S.C. § 102(e) as being anticipated by "Applicant's Prior Art (Figs. 2a/2b)" ("APA"); allowed claims 30-37; objected to claim 39 as dependent upon a rejected base claim, but allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims; withdrew the finality of the previous Office Action of 01/13/2005; and withdrew the previous 35 U.S.C. § 112, first paragraph, rejections of claims 38 and 39, based on the Examiner interview conducted with Appellants' representative on May 17, 2005.

The claims on appeal are set forth in Section IX entitled "Claims Appendix."

IV. STATUS OF AMENDMENTS

Appellants filed a Supplemental Amendment on October 29, 2004, amending claim 38 to include additional language, for which support is found in the claim language as originally filed. This Supplemental Amendment was entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The invention, as recited in independent claim 38, is directed to a semiconductor device comprising: a substrate (*See* item 201, Fig. 22K, and corresponding description in specification on pp. 69-74); a gate wiring layer (*See* item 212, Fig. 22K) formed on one major surface of said substrate; an insulating film (*See* item 210, Fig. 22K) interposed between said substrate and said gate wiring layer and covering a side surface of said gate wiring layer; a pair of thin films formed on one major surface of said substrate, and arranged on two sides of said gate wiring layer (*See* Fig. 22K - "extension(s) 204," located on opposing sides of gate insulating film 210;); and a gate sidewall (*See* item 207, Fig. 22K) formed on said pair of thin films, covering said side surface of said gate wiring layer, and made of an insulator, wherein a region of said pair of thin films between said gate sidewall and said substrate (*See* Fig. 22K - "extension(s) 204," located on opposing sides of gate insulating film 210), a remaining region of said pair of thin films on which said gate sidewall is absent (*See* Fig. 22K - this remaining region is n^+-type diffusion region(s) 208 formed adjacent to extension(s) 204 and on opposing sides of gate insulating film 210; gate sidewall 207 is not present over n^+-type diffusion region(s) 208, and hence is 'absent'), and a surface region of said substrate in contact with the remaining region contain a semiconductor and a conductive impurity.

VI. GROUNDS OF REJECTION TO BE REVIEWED

1. Claim 38 stands rejected under 35 U.S.C. § 102(e) as being anticipated by "Applicant's Prior Art (Figs. 2a/2b)" ("APA").

VII. ARGUMENT

A. Introduction

Each claim of this patent application is separately patentable and, upon issuance of a patent, will be entitled to a separate presumption of validity under 35 U.S.C. § 282. For convenience in handling this appeal, however, the claims will be grouped as follows. All of the claims do not stand or fall together.

1. Allowed claims 30-37 stand or fall together.
2. Regarding the rejection of claim 38 under 35 U.S.C. § 102(e), claim 38 stands alone.
3. Objected-to claim 39 stands alone.

B. Detailed Arguments

1. The rejection of claim 38 under 35 U.S.C. § 102(e) over APA should be reversed.

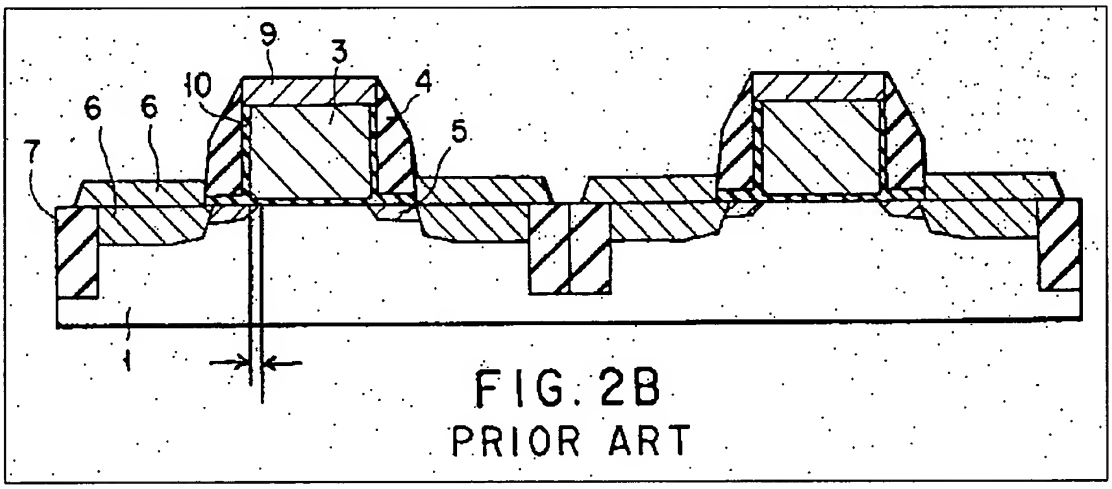
The Examiner's rejection contains clear errors and omits the essential elements necessary for a *prima facie* case of anticipation of Appellants' claim 38.

A proper 35 U.S.C. § 102(e) rejection requires that each and every element of each of the claims in issue be found, either expressly described or under principles of inherency, in a single reference. Furthermore, "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." *See* M.P.E.P. § 2131, quoting *Richardson v. Suzuki Motor Co.*, 868 F.2d 1126, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989).

Since APA does not disclose each and every element of claim 38, the rejection is improper and should be reversed. For the reasons that follow, the Examiner's allegations fail to satisfy the essential elements of a proper anticipation rejection.

The reasoning presented below establishes that at least the elements "a pair of thin films ... arranged on two sides of said gate wiring layer," and "a remaining region of said pair of thin films on which said gate sidewall is absent," both recited in claim 38, are not disclosed in APA.

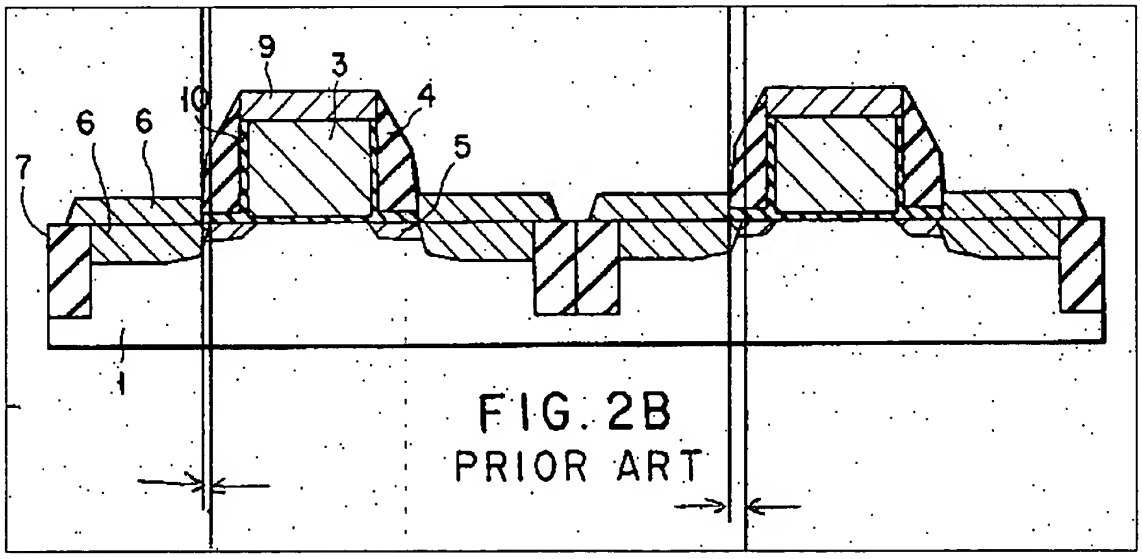
In the 06/03/05 Office Action, the Examiner alleged that APA contains "a pair of thin films (5) ... arranged on two sides of the gate wiring layer" (pp. 2-3). An examination of APA Fig. 2B shows this to be wholly incorrect. In fact, the "pair of thin films (5)" (n-type impurity diffusion region "extension" - p. 1, ll. 22-24) are not arranged on two sides of the gate wiring layer (gate electrode 3) in Fig. 2B. Rather, they are beneath the gate insulating films (unlabeled portion directly below gate electrode 3) and the thermal oxidation film 10. Further, they are even beneath a portion of gate electrode 3. APA Fig. 2B, as presented below in Reference Fig. A, has been annotated to illustrate the overlapping portion of thin films 5 that is beneath the gate insulating films and gate electrode 3. Thus, APA does not disclose "a pair of thin films ... *arranged on two sides of said gate wiring layer*" (emphasis added), according to claim 38.



REFERENCE FIG. A - depicting the portion of thin films 5 beneath gate electrode 3.

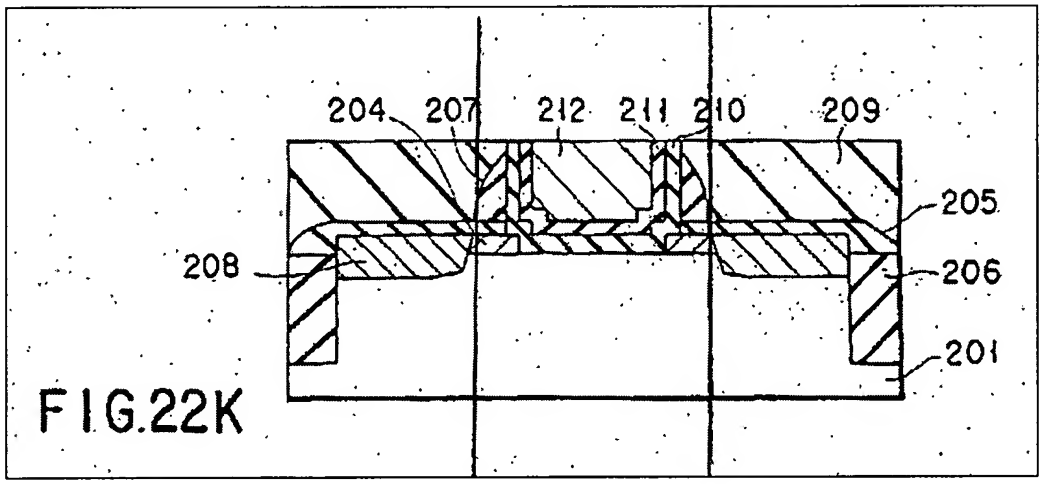
Moreover, in part of the Examiner's allegations on pages 2-3 of the 06/03/2005 Office Action, the Examiner alleges that there exists "a remaining region of [said] pair of thin films (region under diffusion region 6 (area to the left of portion 5 in Fig. 2b)) on which [said] gate sidewall is absent..." An examination of APA Figs. 2A/2B also shows this to be wholly incorrect.

APA Figs. 2A/2B show, for example, that prior art insulating gate sidewall 4 extends beyond the pair of thin films 5 (n-type impurity diffusion region "extension" - p. 1, ll. 22-24) and partially overlaps the top of deeper n^+-type diffusion region 6. To illustrate this clearly, APA Fig. 2B, as presented below in Reference Fig. B, has been annotated to illustrate the overlapping portion of gate sidewall 4 that extends beyond thin films 5, particularly the left side of the rightmost depicted device and the left side of the leftmost depicted device, where insulting gate sidewalls 4 extend partially over the top of deeper n^+-type diffusion region 6. To a lesser extent, this is even depicted on the right side of the leftmost and rightmost device, where the black line representing the outermost region of insulating gate sidewall 4 extends slightly beyond the right of the outer edge of thin film 5. Thus, in the context of APA Figs. 2A/2B, insulating gate sidewall 4 is present over parts of n^+-type diffusion region 6 (e.g., the remaining region of said pair of thin films 5 in Figs. 2A/2B), and hence is not absent. This is different from claim 38, which requires "a remaining region of said pair of thin films on which said gate sidewall is absent" (emphasis added).



REFERENCE FIG. B - depicting the partial overlap of gate sidewall 4 over region 6.

In contrast, an embodiment of Appellants' invention shown in Fig. 22K, corresponding to independent claim 38, shows a gate sidewall 207 that does not at all overlap any of n^+-type diffusion regions 208. *See* Fig. 22K, as presented below in Reference Fig. C, annotated to illustrate that the "remaining region" recited in claim 38, as shown in Fig. 22K, is n^+-type diffusion region(s) 208 formed adjacent to extension(s) 204 and on opposing sides of gate insulating film 210. As indicated by the vertical lines in Reference Fig. C, there is no overlap between gate sidewall 207 and regions 208. Thus, gate sidewall 207 is not present over n^+-type diffusion region(s) 208, and hence is absent. Furthermore, Appellants point out that extension(s) 204 are not beneath gate electrode 212. *See* Reference Fig. C below, and compare with Reference Fig. A, *supra*.



REFERENCE FIG. C - depicting the absence of region(s) 208 over gate sidewall 207.

Thus, a comparison of APA Figs. 2A/2B and the language of independent claim 38 clearly demonstrates that APA does not disclose at least Appellants' claimed "a pair of thin films ... arranged on two sides of said gate wiring layer," and "a remaining region of said pair of thin films on which said gate sidewall is absent," as recited in claim 38.

APA therefore does not anticipate Appellants' independent claim 38. Independent claim 38 is therefore allowable, for the reasons set forth above, and dependent claim 39 (only objected

to as being dependent upon rejected base claim 38) is also allowable at least by virtue of its dependence from allowable base claim 38. Therefore, Appellants request that the improper 35 U.S.C. § 102(e) rejection of claim 38 be reversed.

VIII. CONCLUSION

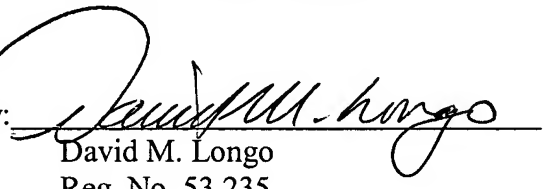
For the reasons given above, pending claims 30-39 are allowable and reversal of the Examiner's rejection is respectfully requested.

To the extent any extension of time under 37 C.F.R. § 1.136 is required to obtain entry of this Appeal Brief, such extension is hereby respectfully requested. If there are any fees due under 37 C.F.R. §§ 1.16 or 1.17 that are not enclosed herewith, including any fees required for an extension of time under 37 C.F.R. § 1.136, please charge such fees to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: November 16, 2005

By: 
David M. Longo
Reg. No. 53,235

IX. CLAIMS APPENDIX

Claims Appendix to Appeal Brief Under Rule 41.37(c)(1)(viii)

30. A semiconductor device comprising:

a substrate;

a device isolation insulating film formed on one major surface of said substrate,

a gate electrode formed on the major surface of said substrate;

a gate wiring layer formed in said device isolation insulating film and connected to said gate electrode;

a source electrode and drain electrode arranged on the major surface of said substrate to face each other via said gate electrode; and

an insulating film covering bottom and side surfaces of each of said gate electrode and said gate wiring layer; and

wherein said gate electrode, said gate wiring layer, said source electrode, and said drain electrode have upper surface levels equal to or lower than an upper surface level of said device isolation insulating film.

31. A device according to claim 30, further comprising a source diffusion layer and a drain diffusion layer below said source electrode and said drain electrode.

32. A device according to claim 31, wherein said gate electrode and said gate wiring layer have bottom surfaces lower than upper surfaces of said source and drain diffusion layers.

33. A device according to claim 30, wherein said gate electrode, said gate wiring layer, and said source and drain electrodes have upper surface levels equal to each other.

34. A device according to claim 30, wherein said gate electrode and said gate wiring layer have upper surface levels lower than upper surface levels of said source and drain electrodes.

35. A device according to claim 30, wherein said gate electrode and said gate wiring layer have upper surface levels higher than upper surface levels of said source and drain electrodes.

36. A device according to claim 30, further comprising a connection wiring layer connected to at least one of said source electrode, said drain electrode, said gate electrode, and said gate wiring layer, said connection wiring layer having an upper surface level equal to or lower than the upper surface level of said device isolation insulating film.

37. A semiconductor device comprising:

a substrate;

a gate wiring layer formed on one major surface of said substrate;

an insulating film interposed between said substrate and said gate wiring layer and covering a side surface of said gate wiring layer;

a pair of thin films formed on one major surface of said substrate, and arranged on two sides of said gate wiring layer; and

a gate sidewall formed on said pair of thin films, covering said side surface of said gate wiring layer, and made of an insulator, wherein a region of said pair of thin films between said gate sidewall and said substrate contains a semiconductor and a conductive impurity, and wherein the region of said pair of thin films between said gate sidewall and said substrate has an upper surface level higher than an upper surface level of a portion of the substrate below the gate wiring layer.

38. A semiconductor device comprising:

a substrate;

a gate wiring layer formed on one major surface of said substrate;

an insulating film interposed between said substrate and said gate wiring layer and covering a side surface of said gate wiring layer;

a pair of thin films formed on one major surface of said substrate, and arranged on two sides of said gate wiring layer; and

a gate sidewall formed on said pair of thin films, covering said side surface of said gate wiring layer, and made of an insulator, wherein a region of said pair of thin films between said gate sidewall and said substrate, a remaining region of said pair of thin films on which said gate sidewall is absent, and a surface region of said substrate in contact with the remaining region contain a semiconductor and a conductive impurity.

39. A device according to claim 38, wherein the region of said pair of thin films between said gate sidewall and said substrate has an upper surface level higher than an upper surface level of a portion of the substrate below the gate wiring layer.

X. EVIDENCE APPENDIX

NONE

XI. RELATED PROCEEDINGS APPENDIX

NONE